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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,753	11/15/2002	Charles S. Chiu	BUR920020064	9185

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EXAMINER	
PHAN, THAI Q	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 01/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,753	CHIU ET AL.	
	Examiner	Art Unit	
	Thai Q. Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,11-15 and 17-20* is/are rejected.

7)☒ Claim(s) *3,10 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 November 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to applicants' amendment filed on 10/10/2005. Claims 1-20 are pending in the Action.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 4-9, 11-15, and 17-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Soudier, C. (US patent application publication no. 2002/0193978 A1).

As per claim 1, Soudier anticipates a method and system for simulating and generating an equivalent power model for an integrated circuit with feature limitations very identical to the claimed invention. According to Soudier, the method includes steps

Generating a partitioned model by partitioning the circuit into a plurality of simulation windows having a similar characteristics or having same parameter settings [0039]-[0042], [0046], [0064],

Applying by converting i/o within each simulation window to a current source and generating the equivalent model for at least one simulation window based on an

observed current change rate of the simulation window as claimed [0063]-[0139]. The simulation window for selecting and setting simulation parameters, simulation file, setting parameters, grid blocks, block interconnection, models for grid computing, etc. The simulation window herein is interactive. It allows user to setting simulation blocks, setting circuit block or grids interconnections, interconnecting simulation blocks or grid blocks, etc for power simulation and verification of a portion or a whole circuit.

As per claim 2, Soudier anticipates steps of simulating operation of the model, and monitoring a current change rate of the simulation window [0063] to [0139],

Converting the current change rate of each simulation window for the I/O of the equivalent model.

As per claims 4-7, Soudier anticipates the claimed limitations for circuit element characteristics such as inductance, capacitance, etc.

As per claim 8, Soudier anticipates a method, system and computer program product having computer readable medium and code for simulating and generating an equivalent power model for an integrated circuit with feature limitations very identical to the claimed invention. According to Soudier, the computer program product includes means for performing:

Generating a partitioned model by partitioning the circuit into a plurality of simulation windows having a similar characteristics [0042],

Applying by converting i/o within each simulation window to a current source and generating the equivalent model for at least one simulation window based on an observed current change rate of the simulation window as claimed [0063]-[0139].

As per claim 9, Soudier anticipates computer program product means for simulating operation of the model, and monitoring a current change rate of the simulation window [0063] to [0139],

Converting the current change rate of each simulation window for the I/O of the equivalent model.

As per claims 11-14, Soudier anticipates the claimed limitations for circuit element characteristics such as inductance, capacitance, etc.

As per claim 15, Soudier anticipates a method and system for simulating and generating an equivalent power model for an integrated circuit with feature limitations very identical to the claimed invention. According to Soudier, the system includes means:

Generating a partitioned model by partitioning the circuit into a plurality of simulation windows having a similar characteristics [0042],

Applying by converting i/o within each simulation window to a current source and generating the equivalent model for at least one simulation window based on an observed current change rate of the simulation window as claimed [0063]-[0139]. These interactive simulation windows herein are for allowing user to setting simulation blocks, setting circuit block or grids interconnections, etc for power simulation and verification ([0029], [0072], [0256]-[0289]).

As per claims 17-20, Soudier anticipates the claimed limitations for circuit element characteristics such as inductance, capacitance, etc.

Allowable Subject Matter

Claims 3, 10 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3, 10 and 16 further require the claimed features of converting to actual i/o based on known current rate changes of i/o and maintaining actual ratios of different types of i/o within each simulation window, which have not been disclosed in the closest prior art of record.

Response to Arguments

Applicant's arguments filed 10/10/2005 have been fully considered but they are not persuasive.

In response to applicants' argument Soudier does not disclose a partitioning step in the simulation process, the examiner does not agree with. Soudier derives a simulation schema by setting and loading a circuit grid model (Fig. 6) or partitioning the circuit into gridding parts for power simulation for instance [0046], [0063]-[0068].

In response to applicants' argument Soudier does not disclose a simulation window as claimed in independent claims, the examiner disagree. As shown in Fig. 17 and in [0029], [0072], [0256]-[0289], Soudier discloses the claimed simulation window for selecting and setting simulation parameters, simulation file, setting parameters, grid blocks, block interconnection, models for grid computing, etc. The simulation window herein is interactive and for allowing user to setting simulation blocks, setting circuit

block or grids interconnections, etc for power simulation and verification. In addition to interfacing, the simulation window in Soudier is for changing simulation parameters, setting interconnection parameters, selecting circuit blocks or gridding, etc for power simulation.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 5,751,592, issued to Takai et al, on 05-1998

2. US patent no. 6,124,143, issued to Sugasawara, Emery, on 09-2000

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is 571-272-3783.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dec. 21, 2005

Thai Phan
Patent Examiner